

Amendments to the Specification:

Please replace the full paragraph beginning on page 3, line 2 and ending on page 4 of the specification with the paragraph below. The paragraph is amended to correct a reference to the pumping capacitor. Added text is underlined and deleted text has been struck through.

The above object has been achieved with a charge pump having improved gain per stage achieved by limiting the influence of threshold voltage and body effect. The present invention features use of PMOS devices to realize switches of an integrated circuit charge pump because the limitations of prior NMOS transistors due to threshold voltage drop and body effect are not present with PMOS switches. Moreover, the voltage difference between all the nodes of PMOS devices never exceeds VDD on the charge pump of the present invention. That way, the thick gate oxide needed for triple wells and N-wells in general is not needed on the charge pump of the present invention. The gain per stage of the charge pump structure of the present invention is very close to VDD and is limited only by parasitics. A charge pump structure of the present invention has a pumping capacitor connected to a pumping node, a first PMOS device connected to an input node, a second PMOS device connected to an output node, a third PMOS device electrically communicating with the first PMOS device, and an auxiliary capacitor connected to the first PMOS device. In this embodiment, the first PMOS device electrically communicates with the ~~coupling~~ pumping capacitor and is configured to connect the pumping node to the input node when the pumping capacitor is not boosted. The second PMOS device electrically communicates with the pumping capacitor and is configured to transfer electrical current from the pumping node to the output node when the pumping capacitor is boosted. At the

same time, the second PMOS device is configured to prevent a reversal current feedback from the output node to the pumping node when the pumping capacitor is boosted. The third PMOS device is configured to switch a gate of the first PMOS device to a boosted pump node potential in order to prevent the current feedback from the pumping node to the input node when the pumping capacitor is boosted. The auxiliary capacitor is configured to generate an under-shoot on the gate of the first PMOS device and to switch the apparatus to an "ON" state when an electrical current is transferred from the input node to the pumping node.

Please replace the full paragraph beginning on page 4, line 15 and ending on page 5 of the specification with the paragraph below. The paragraph is amended to correct a reference to auxiliary capacitor. Added text is underlined and deleted text has been struck through.

In a further embodiment of the present invention, the apparatus for generating a supply voltage internally within an integrated circuit comprises an independently controlled charge pump stage having an input control node, a pumping capacitor connected to a pumping node, a first PMOS device connected to the input control node, a second PMOS device connected to an output control node, and a third PMOS device electrically communicating with the first PMOS device. In this embodiment, the first PMOS device electrically communicates with the ~~coupling~~ pumping capacitor and is configured to connect the pumping node to the input control node when the pumping capacitor is not boosted. The second PMOS device electrically communicates with the pumping capacitor and is configured to transfer electrical current from the pumping node to the output control node when the pumping capacitor is boosted. The second PMOS device is configured to prevent a reversal current feedback from the output control node to the pumping node when the pumping capacitor is not boosted, and the third PMOS device is configured to switch a gate of the first PMOS device to a boosted pump node potential in order to prevent the current feedback from the pumping node to the input control node when the pumping capacitor is boosted. Each substructure further comprises an auxiliary capacitor connected to the first PMOS device. The auxiliary capacitor is configured to generate an under-shoot on the gate of the first PMOS device, and configured to switch the apparatus to an "ON" state when an electrical current is transferred from the input control node to the pumping node.

Please replace the full paragraph beginning on page 11, line 28, and ending on page 12 of the specification with the paragraph below. The paragraph is amended to correct a reference to the pumping capacitor. Added text is underlined and deleted text has been struck through.

After the potential  $\Phi_{\text{aux}}$  switches to VDD (102 of FIG. 3B), the potential at the  $\text{netaux1}$  52 node rises from  $V_{\text{low}}$  to  $V_{\text{in}}$  due to the voltage on ~~coupling~~ auxiliary capacitor 38. Then the potential  $\Phi_1$  (100 of FIG. 3A) switches to VDD, the potential at node 48 rises to  $V_{\text{in}} + V_{\text{DD}}$ , as well as the potential at the node 52 which is connected to node 48 through device 26. At the next phase, the potential  $\Phi_2$  goes low (104 of FIG. 3C), switching the potential at the node 50 to  $V_{\text{in}}$ , and switching the potential at the node 54 to  $V_{\text{in}}$  via device 32. At this point in time, the potential at the node 50 is low and is equal to  $V_{\text{in}}$ . As a result, device 24 turns ON and the charge transfer from the net-pumping node 48 to the output node 44 occurs. However, because device 22 and device 30 have potential on their gates equal to  $V_{\text{in}} + V_{\text{DD}}$ , they are OFF and there is no reversal charge transfer.